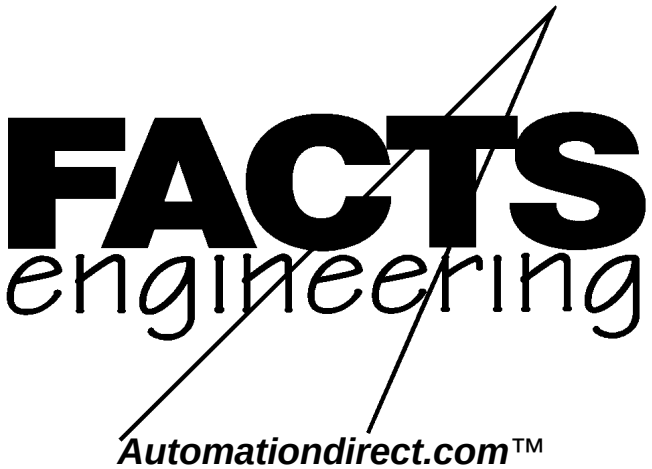

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Direct Logic 305

High Speed Parallel

Bridge CPU

F3-PMUX-1

Manual Order Number: F3-PMUX-1-M

TRADEMARKS

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TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION

305 BRIDGE CPU DESCRIPTION

The High Speed Parallel 305 Bridge CPU™ is a computer input/output (I/O) controller. The Bridge CPU emulates the Opto 22 PAMUX™ parallel communication protocol for digital and analog host computer I/O control. The Bridge CPU is the link between the numerous host computer software packages with PAMUX drivers and the wide range of analog and digital optically isolated industrial I/O modules available for the ***Direct*** Logic 305 programmable controller.

128 POINT I/O DENSITY

A typical system consists of a DL305 five, eight or ten slot base with power supplies. The 305 Bridge CPU plugs into the first slot of the rack. The module directly controls a mix of up to 128 digital and analog I/O points in a single 19" ten slot rack.

COMMUNICATION DAISY CHAIN

305 Bridge CPUs can be daisy chained with Opto 22 PAMUX brain boards and other Bridge CPUs. A Host Computer communicates to the I/O using an 8-bit data bus, and a 6-bit address bus. Connection is made via a 50 pin ribbon cable. A total of four 305 Bridge CPUs may be daisy chained on the same cable for a maximum of 512 digital and analog I/O points. Maximum end to end cable length is 400 feet.

Note: Resistor networks for proper cable termination are included in sockets on the Bridge CPU.

Two methods of daisy chaining or bussing Bridge CPUs are described in Appendix B. Either physical connection method permits removal of any Bridge CPU between the PAMUX master and the last Bridge CPU without disrupting between the host computer and other Bridge CPUs on the bus. The last Bridge CPU must have the termination resistors installed and must be powered before other Bridge CPUs on the network can operate

I/O MODULES NOT SUPPORTED BY THE BRIDGE

Currently the 305 Bridge CPUs support over 36 different ***Direct*** Logic 305 I/O modules. The only Direct Logic modules which are incompatible with the Bridge CPU are listed below.

D3-HSC	High Speed Counter
D3-04AD	Analog Input, 8-bit, 4 points
D3-02DA	Analog Output, 8-Bit, 2 points
F3-08THM-n	Thermocouple Input (call FACTS for availability)

FACTS ENGINEERING 305 BRIDGE COMPARED TO OPTO 22 PAMUX

Replace Up To 8 Brain Boards and Mounting Racks

PAMUX requires a brain board for every 4, 8, 16 or 32 point mounting rack. Separate brain boards are required for digital and analog I/O racks. Each brain board has a unique PAMUX address assigned to it. A PAMUX address supports a maximum of 32 digital or 16 analog I/O points.

The Bridge CPU has 16 consecutive 8 bit addresses assigned to it. Thus it can control a mix of 128 digital and analog I/O. The 305 Bridge CPU uses jumpers to identify I/O modules in the DL305 rack as either digital or analog. To the host computer, each 16 point digital or 16 point analog I/O module slot in the DL305 appears to be a separate PAMUX brain board.

Automatic Module Type Configuration

Inputs and outputs must be identified for the PAMUX brain boards each time there is loss of power.

The 305 Bridge automatically identifies points as inputs or outputs. The Bridge's analog configuration registers can be read to determine the physical configuration of I/O modules at that address.

Built-in Logic and Control Power Supplies

All PAMUX boards require an external +5 VDC power supply. Opto 22 analog I/O modules require an external +15 and -15 VDC power supply.

The 305 Bridge CPU and the DL305 I/O modules are powered directly by the DL305 rack. Analog I/O modules use the 24 VDC power supply built into the DL305 rack to generate ± 15 VDC supplies internally. A separate DC power supply is only needed if required to power external field devices. Since FACTS Engineering 4-20 mA analog output modules source current, an external loop power supply is not required.

CHAPTER 2: INSTALLATION

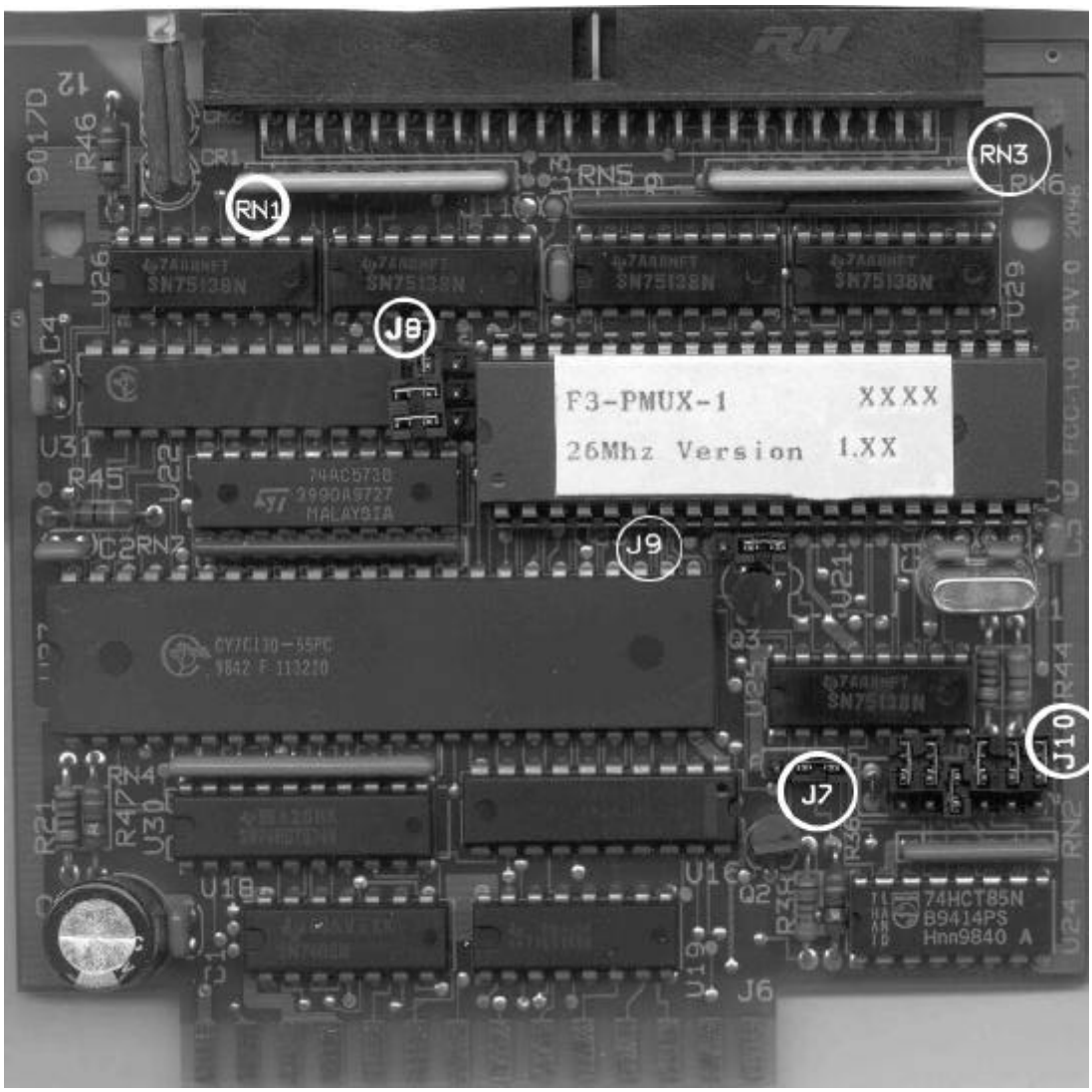
LED INDICATORS

When power is first applied to the base, the RESET LED will come ON. After the power supply has stabilized, the Bridge CPU will turn ON the ADDR LED. Upon successful completion of the internal diagnostic routine, the Bridge will turn OFF the ADDR LED. The ADDR LED will remain ON if the Bridge Base Address is 48 and the cable is OFF.

When the reset line is active the RESET LED will be ON. When the base is running the RESET LED will be OFF. Each read or write to the Bridge CPU will toggle the ADDR LED.

JUMPER LOCATIONS AND TERMINATING RESISTOR NETWORKS

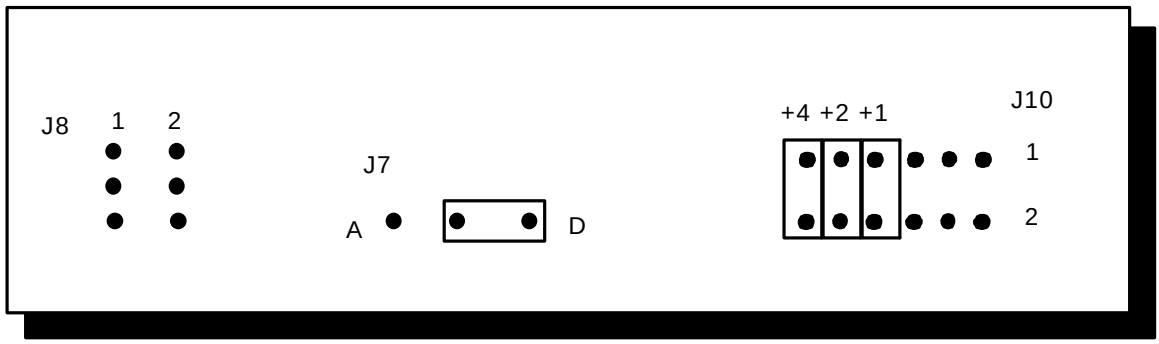
The following graphic shows the position of the four groups of jumpers used to configure the operating mode of the High Speed Parallel Bridge CPU. Also shown are the two resistor networks used for termination, RN1 and RN3.



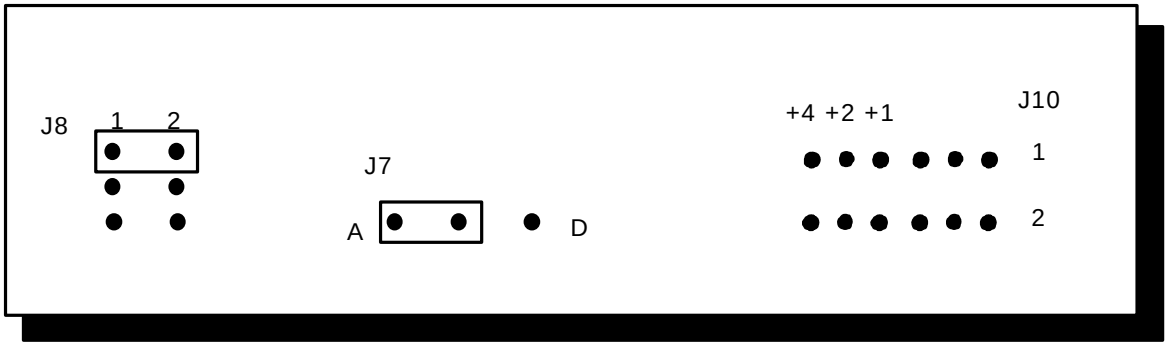
ANALOG AND DIGITAL MODULE SLOT DESIGNATION

Digital and analog modules have slot assignments programmed by installing shunts on jumpers as shown in the following diagrams.

All Slots Digital

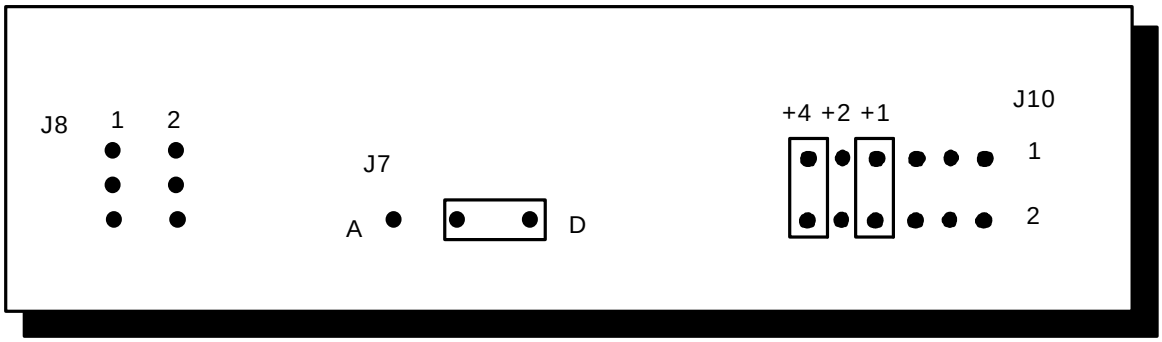


All slots Analog



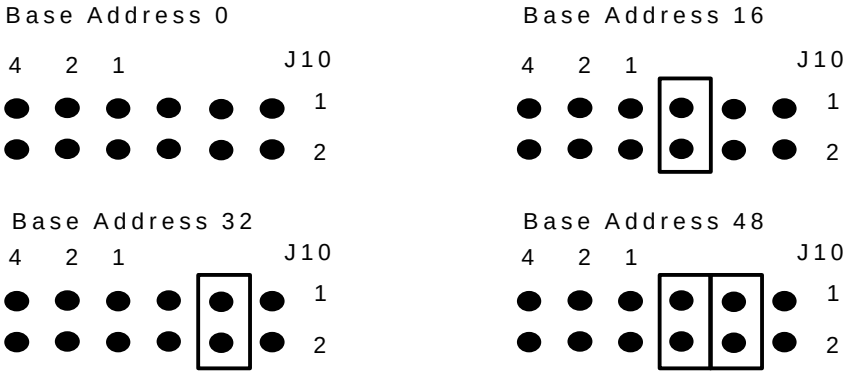
Combination Analog and Digital

The slot next to the Bridge CPU is defined as slot 0. Positioning a J7 shunt on the "D" side will configure slot 0 as a digital slot. This also enables shunts installed at J10 on positions "+1", "+2", and "+4" to select the number of additional consecutive digital slots in the base. All remaining slots are for analog modules. For example, placing a shunt on J5 "+4" and "+1" will configure 6 slots for a digital module (1+4+1 = 6). This leaves slot 6 and slot 7 configured for an analog module.



BRIDGE CPU ADDRESS SELECTION

There are 4 possible 305 Bridge CPU base addresses. Each Bridge CPU on the same daisy chain must be assigned a unique base address. The base address is the address for the I/O module in slot 0 (I/O module next to Bridge CPU). Adjacent DL305 slots are addressed using consecutively even addresses. For example, if the base address is 32 then slot 0 would have 8 I/O positions at address 32 and 8 positions at address 33. Slot 1 would be at addresses 34 and 35. The Bridge CPU base address is selected by the placement of two shunts on J10 as shown in the following diagrams.



A read or write to a slot within a Bridge CPU's address range will cause the "ADDR" LED to flash. Module address = Base Address + Slot Number x 2.

Direct Logic 305 Slot Address Map

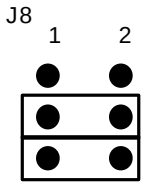
Slot 7		Slot 6		Slot5		Slot4		Slot 3		Slot 2		Slot 1		Slot 0		Bridge	DL305
I	II	I	II	I	II	I	II	I	II	I	II	I	II	I	II		
14	15	12	13	10	11	8	9	6	7	4	5	2	3	0	1	C	Power
30	31	28	29	26	27	24	25	22	23	20	21	18	19	16	17	P	Supply
46	47	44	45	42	43	40	41	38	39	36	37	34	35	32	33	U	
62	63	60	61	58	59	56	57	54	55	52	53	50	51	48	49		

"I" = First 8 Digital I/O -or- Analog Data Register
"II" = Second 8 Digital I/O -or- Analog Internal Register Address

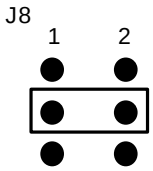
DIGITAL WATCHDOG TIMEOUT ACTION

The action taken by the Bridge CPU following a watchdog timeout is determined by the position of shunts on two jumpers located at J8. A watchdog timeout will occur if the host computer fails to read or write to a slot within the Bridge CPU's address range within a preset time limit. The default timeout for digital slots is 2 seconds. A single watchdog timeout value is set for each Bridge CPU. The default digital timeout maybe changed via software as described below.

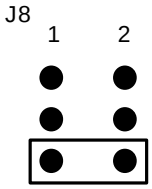
Watchdog Timeout Disabled



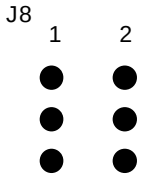
Turn ON 1st output in 1st digital module and retain state of all other digital outputs



Turn OFF all digital outputs



Turn ON 1st output in 1st digital module and turn OFF all other outputs



RESISTOR NETWORK USAGE

The resistor networks labeled RN1 and RN3 terminate the ribbon cable connection.

If several F3-PMUX CPUs are daisy chain connected on a single ribbon cable then both resistor networks must be removed from all Bridge CPUs which are intermediate drops on the ribbon cable.

Leave both resistor networks installed on the furthest Bridge CPU from the host computer or if only a single F3-PMUX is used.

HEADER CONNECTOR PIN OUT

The Bridge CPU bus consists of 8 data, 6 address lines, plus a read, a write and a reset line. The two most significant address lines A4 and A5 select 1 of 4 Bridge CPU bases. The other four address lines select 1 of 16 8-bit addresses.

The 8 data lines are used to read or write the group of 8 digital I/O selected by the address lines. The data lines are also used to multiplex the address and data for the analog internal registers.

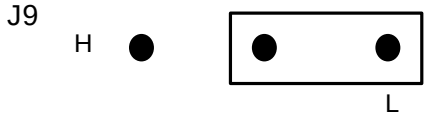
Pin	Symbol	Description
1	A0	Address line 0 (least significant)
3	A1	Address line 1
5	A2	Address line 2
7	A3	Address line 3
9	A4	Address line 4
11	A5	Address line 5
13	WR	High to low transition Writes data
15	RD	High to low transition Reads data
33	D7	Data line 7 (most significant)
35	D6	Data line 6
37	D5	Data line 5
39	D4	Data line 4
41	D3	Data line 3
43	D2	Data line 2
45	D1	Data line 1
47	D0	Data line 0 (least significant)
49	RST*	Reset pulse line

All even numbered pins are connected to logic ground. Pins 17,19,21,23,25,27,29, and 31 are not connected. All signals except RST* are active high. RST active level is jumper selectable.

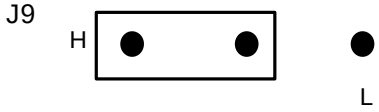
RESET LEVEL

The three post jumper next to the CPU, J9, is used to select the active level of the RST line. The module is shipped from the factory in the active low position (towards the crystal). Move the J9 jumper to the "H" position to change the reset pulse line to active high.

Active Low Reset



Active High Reset

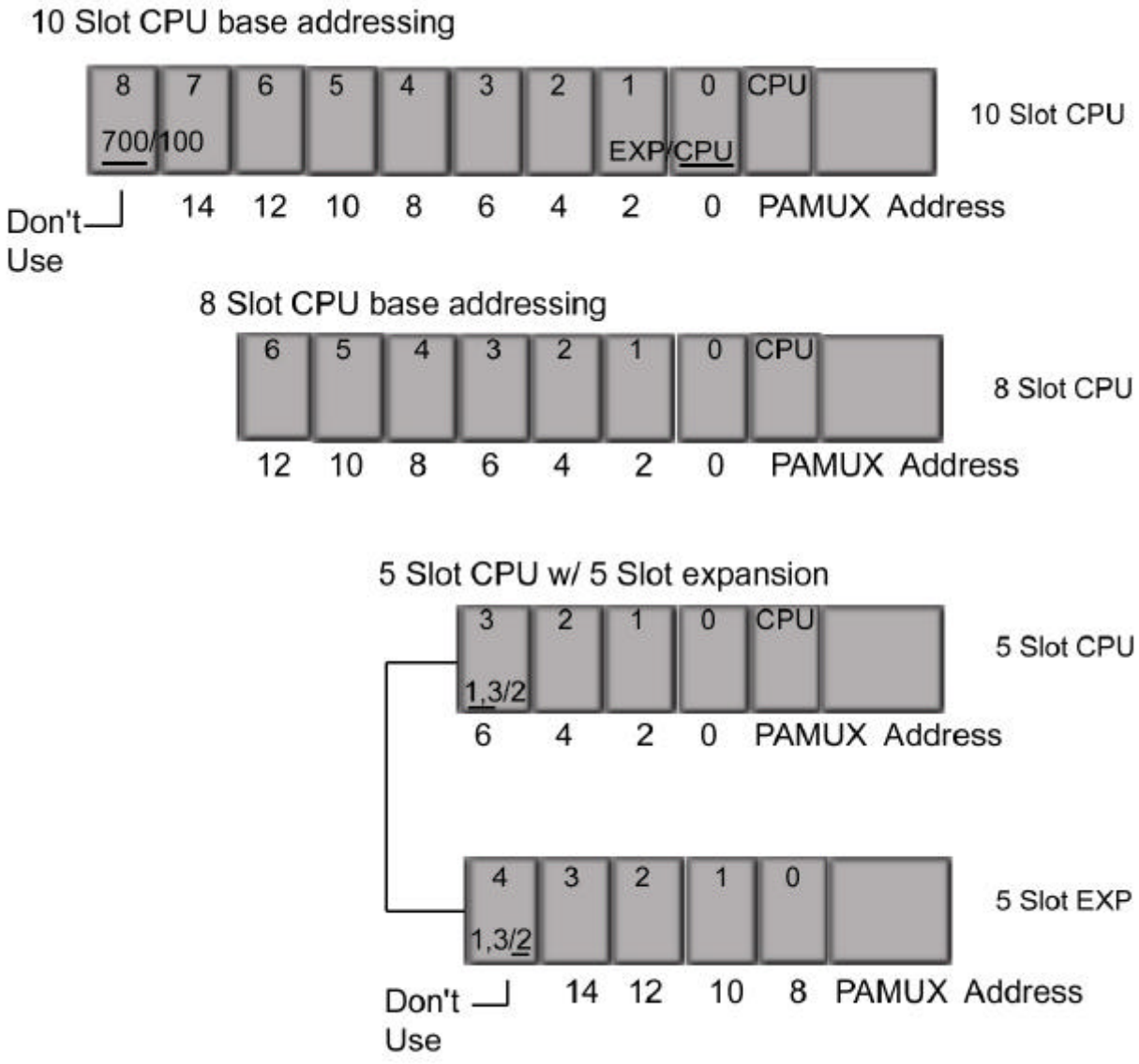


BASE JUMPER SETTINGS AND ADDRESSING

Direct Logic 305 10-slot racks have configuration switches on the back plane which must be set for correct operation. Set the "SW1" jumper to the "CPU" position. The position of the "SW2" jumper does not matter since the last slot is not used.

If two 5-slot bases are used, the switch in the CPU base must be in the "1-3" position. The switch in the expansion base should be in the "2" position.

Please refer to the PLC ***Direct*** manual for DL305 installation instructions and mounting dimensions.



CHAPTER 3: READING AND WRITING THE BRIDGE

GENERAL DESCRIPTION

Access to the Bridge CPU is through high speed dual port RAM. The Bridge CPU continually reads and updates the dual port RAM. The bus timing specified in Appendix A and the Bridge CPU hardware guarantees that both the Bridge CPU and the host computer may simultaneously access the same dual port memory byte without data corruption.

Each digital and analog module slot takes up two addresses.

The analog internal register address is multiplexed on the data lines.

DIGITAL READ/WRITE

Digital module addresses are:

ModuleAddress = BaseAddress + SlotNumber x 2

ModuleAddress = 1st 8 I/O points (Group "I")

ModuleAddress + 1 = 2nd 8 I/O points (Group "II")

Example BASIC program to read status of 16 inputs in slot 3, 2nd base.

```
'Card = IO address of parallel port
BaseAddress = 16 + Card
Slot = 3
LowInSlot3 = INP(BaseAddress + Slot x 2)
HighInSlot3 = INP(BaseAddress + 1 + Slot x 2)
```

BASIC program to turn ON outputs 1, 2 & 7 and turn OFF outputs 0, 3-6 in slot 1, Group "I", 1st base.

```
'Card = IO address of parallel port
BaseAddress = 0 + Card
Slot = 1
Value = 2 + 4 + &H80
OUT BaseAddress + Slot x 2, Value
```

PROGRAMMING THE DIGITAL WATCHDOG TIMEOUT

First enable the digital watchdog timeout function by positioning shunts at "J8" (see page 4). Next, follow the procedure below to change the timeout from the power-up default of 2 seconds. Note that there is one timeout value for all analog and digital modules in the base. Thus setting an analog watchdog timeout value as described on page 6 will override a digital watchdog timeout. The following procedure can be used when there are no analog modules in the base.

1) Put the Bridge CPU into reset ("RESET" light will be on).

2) Output a value 1 to 65534 to a digital slot in the Bridge CPU base. This value is in 10 millisecond units and will be loaded into the watchdog timer. The value must be output most significant byte first (MSB) and least significant byte second (LSB). Also the LSB must not be zero.

3) The digital watchdog timeout may be set at any digital slot. Write MSB at "II" address and LSB at "I" address (see address map on page 5).

4) Read back the digital value. Both the LSB and MSB will be equal to 255 after the Bridge has loaded the timeout.

5) Put the Bridge into run ("RESET" light will go off).

Example

```
RST = &H2E0                                 'Address of reset line
Card = &H0180                                   'IO address of card in IBM PC
BaseAddress = 0                             'BaseAddress = 0,16,32, or 48
Slot = 0                                    'First module is digital
OUT RST, 0                                  'RESET the Bridge
TimeOut = 2.5                               'Let time-out = 2.5 seconds
TimeOut = TimeOut/.01                           'Convert to 10 msec units
MSB = INT(TimeOut/256)                      'Get MSB
LSB = TimeOut AND &H0FF                     'Get LSB
IF LSB=0 THEN LSB=1                             'LSB can't be 0
ModuleAddress = Card+BaseAddress+Slot*2     'Address of module in base
OUT ModuleAddress+1, MSB                    'Output MSB first
OUT ModuleAddress, LSB                      'Output LSB second

WaitForTimeoutLoad:
IF INP(ModuleAddress+1) <> 255 THEN WaitForTimeoutLoad
IF INP(ModuleAddress) <> 255 THEN WaitForTimeoutLoad
OUT RST, 1      'RUN the Bridge CPU

' Main program loop starts here
```

LOW LEVEL ANALOG MODULE ADDRESSING

This section describes the addressing of analog I/O modules. This information is provided so that you can write your own program to read and write Parallel Bridge CPU Analog I/O. If you are using a program or driver which can already access PAMUX Analog I/O then you may skip this section and continue with "High Level Analog Module Addressing" beginning on page 9.

To access analog module internal data, first place the module's base and slot address plus one (ModuleAddress + 1) on the address bus. Then write to this address (place on the data bus) the address of the internal data register which you wish to access. The Bridge CPU hardware will latch in this address. Now place the module's base and slot address (ModuleAddress) on the address bus and read or write the internal data register. Analog module addresses are:

ModuleAddress = BaseAddress + SlotNumber x 2

ModuleAddress + 1 = Internal Register Address (from table on page 13)

ModuleAddress = Data Register Address (data to/from Internal Register)

Although the Bridge CPU supports the PAMUX semaphore register method of gaining and releasing access to dual port memory, no "gain/release access" is required with the Bridge.

After setting a new analog output value, the Bridge CPU sets the 5th bit of the most significant byte (MSB) of the output value. Thus, the host computer must write the MSB of analog output data even if only the LSB has changed. The new analog output flag allows the Bridge CPU to efficiently set all the analog outputs in one scan.

Analog Module BASIC Program Read Example

Example

```
'READ analog input channel 8, slot 5, last base.
'Card = IO address of parallel port
BaseAddress = 48 + Card
Slot = 5
ModuleAddress = BaseAddress + Slot x 2

RETRY:
OUT ModuleAddress + 1, &H0F             'point to MSB channel 8
MSBCH4 = INP(ModuleAddress)       'get MSB
OUT ModuleAddress + 1, &H0E             'point to LSB channel 8
LSBCH4 = INP(ModuleAddress)       'get LSB
OUT ModuleAddress + 1, &H0F             'point to MSB channel 8
'Bridge update, retry
IF INP(ModuleAddress) <> MSBCH4 THEN RETRY
Value = MSBCH4 * 256 + LSBCH4     '12-bit value is 0-4095
```

Analog Module BASIC Program Write Example

Example WRITE analog channel 4, slot 7, 3rd base address.

```
'Card = IO address of parallel port
BaseAddress = 32 + Card
Slot = 7
ModuleAddress = BaseAddress + Slot x 2
LSBCH7 = VALUE AND &H0FF            'strip off the low byte
MSBCH7 = INT(VALUE/256)     'pick off the high byte
OUT ModuleAddress + 1, 6        'point to LSB channel 4
OUT ModuleAddress, LSBCH7  'write LSB
OUT ModuleAddress + 1, 7        'point to MSB channel 4
OUT ModuleAddress, MSBCH7 'write MSB, cause conversion
```

More About Reading Analog Inputs

As seen in the previous example, an extra step is required to read 12-bit analog input values. One of the following two methods may be used to insure that the two byte values are read properly by the host computer. The first method is recommended for new software applications. The second method is provided for compatibility with existing PAMUX software drivers.

1) The most significant byte of an analog input may be read twice to insure that the Bridge did not write a new 16-bit word while the least significant byte was being read by the host (Bridge is faster than host and writes MSB then LSB).

   Theory: The Bridge CPU could update the MSB and LSB of the analog input after the host reads the MSB but before it reads the LSB. Thus the host should read MSB LSB MSB until both MSB reads match.

2) Reliable dual port memory reads may also be achieved by reading the semaphore register before reading each analog input. This register will return a value < 128 when the Bridge CPU is not updating the analog inputs. Unlike the PAMUX B6 brain board, you do not have to "release access" when you have finished reading the analog inputs. Also you do not have to "gain access" to write analog outputs.

   Theory: The Bridge CPU sets the semaphore register before updating analog inputs. The semaphore register is cleared after the new input word has been written by the Bridge. If the host computer is slow enough, it is possible that the Bridge could set the semaphore register and write both the MSB and LSB of analog data after the host had read the MSB but before it had read the LSB. For this reason, method 1 is recommended.

ANALOG INTERNAL REGISTER ADDRESS MAP

Register Address	Byte	Description	Register Address	Byte	Description
0	L	Analog Channel 1	20	L	Watchdog Value Ch. 1
1	H		21	H	
2	L	Analog Channel 2	22	L	Watchdog Value Ch. 2
3	H		23	H	
4	L	Analog Channel 3	24	L	Watchdog Value Ch. 3
5	H		25	H	
6	L	Analog Channel 4	26	L	Watchdog Value Ch. 4
7	H		27	H	
8	L	Analog Channel 5	28	L	Watchdog Value Ch. 5
9	H		29	H	
A	L	Analog Channel 6	2A	L	Watchdog Value Ch. 6
B	H		2B	H	
C	L	Analog Channel 7	2C	L	Watchdog Value Ch. 7
D	H		2D	H	
E	L	Analog Channel 8	2E	L	Watchdog Value Ch. 8
F	H		2F	H	
10	L	Analog Channel 9	30	L	Watchdog Value Ch. 9
11	H		31	H	
12	L	Analog Channel 10	32	L	Watchdog Value Ch.
13	H		33	H	10
14	L	Analog Channel 11	34	L	
15	H		35	H	Watchdog Value Ch.
16	L	Analog Channel 12	36	L	11
17	H		37	H	
18	L	Analog Channel 13	38	L	Watchdog Value Ch.
19	H		39	H	12
1A	L	Analog Channel 14	3A	L	
1B	H		3B	H	Watchdog Value Ch.
1C	L	Analog Channel 15	3C	L	13
1D	H		3D	H	
1E	L	Analog Channel 16	3E	L	Watchdog Value Ch.
1F	H		3F	H	14
					Watchdog Value Ch. 15
					Watchdog Value Ch. 16

Register Address	Byte	Description
42		Semaphore Register (overlaps with 82 for PAMUX compatibility)
77		Bridge CPU firmware revision number (Read Only)
7A	L	Timeout value for Watchdog Timer
7B	H	
7C		Status Flags (Bit 0=Reset, Bit 1=New Data, Bit 2=WDT)
7D		FE = Analog Module (Read Only)
7E	L	00=Input Type Module, FF=Output Type Module (Read Only)
7F	H	

Notes: All other memory locations are reserved for future use. In the table, H = High data byte, L = Low data byte

ANALOG WATCHDOG TIMEOUT ACTION

A watchdog timeout will occur if the host computer fails to read or write to a slot within the Bridge CPU's address range within a preset time limit.

After a reset, the default for analog slots is no timeout. Setting the analog timeout value enables the analog watchdog timeout function.

A single watchdog timeout value is set for each Bridge CPU. If the digital watchdog timeout function is enabled then the analog timeout value replaces the digital timeout value.

Setting the Analog Watchdog Timeout

The timeout value for the analog watchdog timer is set by writing a value from 1 to 65535 at analog internal register addresses &H7A (LSB) and &H7B (MSB). The timeout value is in 10 millisecond units (2.5 seconds/.01 msec = value = 250).

```
Example     BaseAddress = 0 + Card          'Card = IO address of parallel port
            Slot = 7
            ModuleAddress = BaseAddress + Slot x 2
            VALUE = 1.0/.01                 'value for 1 second timeout
            LSB = VALUE AND &H0FF           'strip off the low byte
            MSB = INT(VALUE/256)            'pick off the high byte
            OUT ModuleAddress + 1, &H7A         'point to LSB time limit
            OUT ModuleAddress, LSB          'write LSB
            OUT ModuleAddress + 1, &H7B         'point to MSB time limit
            OUT ModuleAddress, MSB          'write MSB
```

Setting the Analog Output Level if a Timeout Occurs

After an analog watchdog timeout has occurred, all analog outputs are set to a predetermined level. By default all outputs are set to zero. Each channel may be programmed for any analog output value. Watchdog timeout output levels are set by writing watchdog values into analog internal register addresses &H20 to &H3F.

```
Example     VALUE = 4095  'value for full scale output
            LSB = VALUE AND &H0FF           'strip off the low byte
            MSB = INT(VALUE/256)            'pick off the high byte
            OUT ModuleAddress + 1, &H2A         'point to LSB for Channel 6
            OUT ModuleAddress, LSB          'write LSB
            OUT ModuleAddress + 1, &H2B         'point to MSB for Channel 6
            OUT ModuleAddress, MSB          'write MSB
```

STATUS FLAGS

The status flags are at analog internal register address &H7C.

Bit 0; 1 = RESET 0 = RUN
Bit 1; 1 = NEW DATA 0 = SAME DATA
Bit 2; 1 = TIMEOUT 0 = NO TIMEOUT

The RESET, NEW DATA and TIMEOUT (watchdog timeout) status flags only need to be read for one analog module in each bridge base.

All flags are set by the Bridge CPU and cleared by the host computer.

Reset

Status flag RESET is set to a one during the Bridge CPU power-up/reset cycle. When the Bridge CPU is reset due to loss of power or a signal from the host the, RESET flag is set. This indicates that all analog and digital outputs have been set 0.

```
Example     OUT ModuleAddress + 1, &H7C          'point to Status Flag Reg
            Status = INP(ModuleAddress)          'get Status Byte
            IF (Status AND 1)=0 THEN ForgeAhead
            'clear the RESET flag
            OUT ModuleAddress, Status AND &HFE
            GOSUB StartUpRoutine                 're-initialize watchdog
            ForgeAhead:          'Bridge has not been reset
```

New Data

Status flag NEW DATA is set each time an analog update occurs. This indicates that an analog input or output channel has been read or written by the Bridge.

```
Example     OUT ModuleAddress + 1, &H7C          'point to Status Flag Reg
            Status = INP(ModuleAddress)    'get Status Byte
            IF (Status AND 2)=0 THEN SkipOldData
            'clear the NEW DATA flag
            OUT ModuleAddress, Status AND &HFD

            SkipOldData:                   'Bridge has no new data
```

Timeout

Status flag TIMEOUT is set when the host computer has failed to access the Bridge CPU within the preset time limit (to set the analog watchdog time limit see page 6). This indicates that all digital and analog outputs have been set to their watchdog timeout value.

Application Tip If a Bridge CPU base does not contain any analog modules, an unused slot can be configured for an analog module. This permits changing the digital watchdog timeout without resetting the base. Also the RESET and TIMEOUT Status Flags can be used to determine when digital outputs have been reset due to loss of power or lack of host communication.

CHECKING ANALOG AND DIGITAL SLOT CONFIGURATION

All slots which are hardware selected for an analog module return same firmware version at analog internal register address &H77.

Example

```
Card = &H0180            'IO address of card in IBM PC
BaseAddress = 0          'BaseAddress = 0,16,32, or 48
Version = 102    'Firmware version 1.02
FOR Slot = 0 TO 7
ModuleAddress = Card + BaseAddress + Slot * 2
OUT ModuleAddress + 1, &H77
Value = INP(ModuleAddress)
OUT ModuleAddress + 1, &H7D
MdlType = INP(ModuleAddress)
IF Version=Value THEN
  IF MdlType=254 THEN
    PRINT "Analog in Slot ";Slot;" is ";
        OUT ModuleAddress + 1, &H7E
        IOType = INP(ModuleAddress)
        IF IOType = 0 THEN
          PRINT "INPUT"
        ELSE
          PRINT "OUTPUT"
        END IF
  ELSE
    PRINT "Jumper on J8 if all 8 modules are analog"
  END IF
ELSE
  PRINT "Digital in Slot ";Slot
END IF
NEXT Slot
```

HIGH LEVEL ANALOG MODULE ADDRESSING

Addressing of all 4 channel analog modules are different than the 8 and 16 channel analog input modules. These modules have discrete channel identification bits whereas the 8 and 16 channel analog input modules use binary coded channel identification.

In the following tables, the first analog point of the Host Channel ID is 1. Some software packages refer to the first analog point as 0. In the tables, the first analog point is referred to as Analog Position 0.

F3-04ADS Addressing

Analog Channel	Host Channel ID	Analog Position	I/O Point Mask
1	2	1	0002
2	3	2	0004
3	5	4	0010
4	9	8	0100

F3-04DA-1, F3-04DAS, F3-08AD, F3-08TEMP and F3-16AD Addressing

Analog Channel	Host Channel ID	Analog Position	I/O Point Mask
1	1	0	0001
2	2	1	0002
3	3	2	0004
4	4	3	0008
5	5	4	0010
6	6	5	0020
7	7	6	0040
8	8	7	0080
9	9	8	0100
10	10	9	0200
11	11	10	0400
12	12	11	0800
13	13	12	1000
14	14	13	2000
15	15	14	4000
16	16	15	8000

APPENDIX A - READ/WRITE BUS TIMING

READ/WRITE TIMING AND CABLE LENGTH

Address and data setup times (pulse width of read and write lines) restrict the maximum Bridge CPU 50-pin cable length. A minimum read and write strobe of 2 usec is required for a 300 foot cable.

DUAL PORT MEMORY ARBITRATION AND READ/WRITE TIMING

A minimum read strobe of 1.5 usec is required to guarantee that host byte reads and writes are valid. If the Bridge CPU begins to write a dual port location *before* the host starts to read it and the host read strobe is greater than 1.5 usec then the Bridge will finish the write before the host read strobe correctly latches the data. If the host read strobe is less than 1.5 usec then the host will not reliably read the data. Encase the host read strobe must be less than 1.5 usec wide then the host software should read all byte locations until two successive reads match.

If the Bridge CPU begins to write a dual port location *after* the host starts to read it then the Bridge CPU will be prevented from changing the location until the host has completed the read.

The arbitration logic for the dual port ram is symmetrical. If the host write strobe is greater than 1.5 usec then the host reliably writes data to the dual port. If the host write strobe is less than 1.5 usec then the host should verify a write by reading back the data.

In all cases the hardware prevents data which is being written from being corrupted.

Dual Port Ram Arbitration Logic Summary

Host Computer	Bridge CPU	Result of Simultaneous Dual Port Access
READ	READ	BOTH READ DATA
READ	WRITE	LOSER PREVENTED FROM WRITING IF LOSER IS READING, DATA MAY NOT BE READ CORRECTLY
WRITE	READ	
WRITE	WRITE	WINNER WRITES, LOSER PREVENTED FROM WRITING

WINNER is first to access a ram location, LOSER is second to access the location.

APPENDIX B - CONNECTORS AND CABLING

CONNECTORS

The following ribbon cable connectors may be used for single and daisy chained Bridge CPU installations. Daisy chain Bridge CPUs using either of the sockets shown below. Make a single ribbon cable with a socket crimped onto it at each Bridge CPU position.

Sockets for Direct Connection to Bridge CPU

Part Number	Description
3425-6000	50 CONTACT **SOCKET**, OPEN ENDED FOR BUSSING, 3M
3448-3050	STRAIN RELIEF FOR 3425 SERIES, 3M
1-746195-2	50 CONTACT **RECEPTACLE**, CENTER POLARIZED, AMP
499252-4	STRAIN RELIEF FOR 1-746195-2, AMP

Bridge CPUs may also be daisy chained by crimping a pin or plug connector near the end of each ribbon cable. This cabling method allows each Bridge CPU to have a separate length of ribbon cable (requires 2 sockets and 1 plug connector).

Plugs for Extending a Bridge CPU Bus

Part Number	Description
4650-6001	50 CONTACT **PLUG**, W/O MOUNTING FLANGE, 3M
3448-4650	STRAIN RELIEF FOR 4650-6001, 3M
1-746492-1	50 PIN CONNECTOR, W/O MOUNTING FLANGE, AMP
1-746362-1	STRAIN RELIEF FOR 1-746492-1, AMP

RIBBON CABLE

Part Number	Description
3365/50	28 AWG, 7/36 STRANDED, 100' OR 300' REEL, 3M
3539/50	28 AWG, 19/40 STRANDED, FLEX LIFE, 100' REEL, 3M
3353/50	28 AWG, 7/36 STRANDED, GROUND PLANE, 100' REEL, 3M
3603/50	28 AWG, 7/36 STRANDED, JACKETED, 100' REEL, 3M
3517/50	28 AWG, 7/36 STRANDED, JACKETED/SHIELDED, 100' REEL, 3M
3759/50	28 AWG, 7/36 STRANDED, ROUND JACKETED, 100' REEL, 3M (FOLDED CONSTRUCTION PERMITS MASS TERMINATION EVERY 2.4")
3659/50	28 AWG, 7/36 STRANDED, ROUND JACKETED/SHIELDED, 100', 3M
499116-6	28 AWG, 7/36 STRANDED, 100' REEL, AMP

APPENDIX C - DUAL PORT UPDATE SPEED

DIGITAL I/O

When the Bridge CPU encounters an output module it reads the contents of the appropriate dual port ram location and then updates the status of the modules outputs. When the Bridge CPU encounters an input module it reads the status of the modules inputs and updates the contents of dual port ram. The maximum time required to update all 128 discrete I/O points is .6 msec (26 MHz Dallas 87C520 CPU). Unused slots should be configured as analog points for minimum update times.

ANALOG INPUTS

Every I/O scan one channel of each analog input module in the Bridge CPU base is updated. The time required by the Bridge CPU to convert, read and update the dual port memory for all 32 channels of eight four channel analog input modules is 4 msec. The update time for 64 channels of eight channel input modules is 8 msec. The time required to update all the channels on a single multichannel analog input module is 1 msec times the number of channels scanned. For minimum update times, analog input modules should be jumped to only scan the channels actually being used.

ANALOG OUTPUTS

Analog outputs are updated when the MSB of the value in dual port memory associated with a particular output is changed by the host. Multiple analog outputs on the same analog output module may be simultaneously changed by the host. All changed analog outputs are set by the Bridge CPU during the same I/O update. The additional time to update analog output channels is 100 microseconds for each output changed by the host.